

Arsh Sharma

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EDUCATION

- **National Institute of Technology(NIT) Hamirpur** Himachal Pradesh, India
Integrated B.Tech & M.Tech in Electronics and Communication Engineering(VLSI) CGPI: 8.56
- **Mount Carmel School**
12th - ISC; Percentage: 91% 2018

PROFESSIONAL EXPERIENCE

- **NVIDIA**
ASIC Intern
 - Supporting the power characterization infra for the Post-Silicon Solutions Group.
 - Scripting in Python/shell to automate power characterization and bring up flows for the latest Nvidia GPU and Tegra™ SoC architectures
 - Automated the triggering, power/temperature measurement and data collection for NVIDIA's In-System Test architecture to leverage power as a service to various consumers.
- **Zellerfeld R&D GmbH** Hamburg, Germany
Software Developer
 - Developed tools in Python & Julia Language to support processing, slicing and GCODE generation of complex footwear 3D models and a backend to expose the tooling for a no-code interface.
 - Wrote scripts using FFMPEG for realtime video monitoring and analysis of the 3D printers including the overall print process.

PROJECTS

- **Masters Dissertation**
Studied the physical design flow from RTL(logic) to GDSII(layout).
 - Developed a Julia based tool for the Analytical Placement method with an overall goal of improving the performance of Place & Route in mind.
- **Digital Design and Verification**
Designed FSM, HDL(verilog) implementation and verification environment for:
 - Basic Circuits: Adder, Comparator, Counter, ALU etc.
 - Protocols: UART, SPI, I²C etc.
 - Developed simple as well as Universal Verification Methodolgy(UVM) based testbenches in SystemVerilog.
- **Miscellaneous**
Scripting/Programming based projects
 - Performed High Level Synthesis of a 2nd order Differential Equation solver.
 - **IBMQJulia.jl** A set of scripts to parse Yao.jl based quantum circuits to the IBM-Quantum spec(actual quantum computers). Implemented the OpenQasm specifications paper composing two major units, the REST API and the Yao IR to QObj parser.

SKILLS

- **Languages:** Verilog, System Verilog, Julia, Python, C++, Shell scripting
- **Tools:** GTKWave, Linux, GIT(Version Control), Tools from Cadence/Synopsys
- **Interests:** Functional Verification, FPGA, Computer Architecture, VLSI, Object Oriented Programming(OOPS)

SIDE QUESTS

- **Speaker at ECEConnect 2022:** Gave a talk on software development and open-source software in the context of Electrical Engineering.
- **Speaker at JuliaCon 2021:** Presented my work on Javis.jl to a global community of Julia enthusiasts, developers, scientists and industry. [Link to the talk](#)